REMARKS

Claims 1-6, 8-16 and 21 are pending in the application.

Claims 16 and 21 are allowed.

Claims 1, 2, 4-6, 8 and 10 have been rejected.

Claims 3, 9 and 11-15 are objected to

Claim 1 has been amended, as set forth herein.

Reconsideration of the claims is respectfully requested. The Applicants make the aforementioned amendments and subsequent arguments to place this application in condition for allowance. Alternatively, the Applicants make these amendments and offer these arguments to properly frame the issues for appeal.

I. REJECTION UNDER 35 U.S.C. § 102

Claims 1-2, 4-6, 8 and 10 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,526,495 to *Sevalia, et al* (hereinafter "Sevalia"). The rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Currently amended Independent Claim 1 recites "[a] memory device comprising: a. a memory having at least two predetermined register memory sections addressable by respective address ranges; b. at least one access port for providing access to said memory; c. access control means for addressing said memory so as to operate said register memory sections as shift registers and to map shift register accesses of said at least one access port to predetermined addresses in a global address space of said memory, said control means being external to said memory and being configured to generate memory addresses for writing to and reading from

said memory, and d. **a buffer memory coupled** to said at least one access port and **to said memory**, wherein a line width of said buffer memory and said memory is selected to be greater or equal the data width of said at least one access port multiplied by the sum of read accesses and write accesses per cycle.

The Office Action argues that *Sevalia* (Abstract and col. 1, lines 25-36) teaches a memory having at least two predetermined register memory sections addressable by respective address ranges. The cited portions of *Sevalia* describe the circuit 100 illustrated in Figure 1. For example, the Abstract states "[a] circuit comprising a memory array and a control circuit." Further, column 1, lines 25-27, states "a circuit comprising a memory array and a control circuit. The memory array comprises a plurality of storage queues." Thereafter, *Sevalia*, starting at column 2, line 8, states, "[the] circuit 100 generally comprises a number of storage queues 102a-102n, ... [and] a configuration register 107." Therefore, the Office Action argues that the *Sevalia* circuit 100 with storage queues 102a-102n teaches the "memory having at least two predetermined register memory sections addressable by respective address ranges" as recited in independent Claim 1.

First, *Sevalia* does not teach or suggest a "memory having at least two predetermined register memory sections addressable by respective address ranges" as contended by the Office Action. The plurality of storage queues (102a-102n) are First In First Out (FIFO) storage elements. (See *Sevalia*, col. 2, lines 18-14). *Sevalia* contains no disclosure that the FIFO storage elements (102a-102n) are "addressable by respective address ranges." Reading and writing to the FIFO storage elements (102a-102n) are controlled by control signals (e.g., R/WA-R/WD). (See *Sevalia*, Figure 5 and col.4, lines 12-23). *Sevalia* states that the "read and write control signals R/WA-R/WD may control reading and writing to/from the FIFO queues." *Sevalia* does not disclose addressing or addressable ranges. Accordingly, *Sevalia* does not teach or suggest "a memory having at least two predetermined register memory sections addressable by respective address ranges" as recited by independent Claim 1.

The Office Action further argues that *Sevalia* (col. 2, lines 18-38) teaches a buffer memory connectable to at least one access port and to the memory, wherein a line width of said buffer

memory and said memory is selected to be greater or equal the data width of said at least one access port multiplied by the sum of read accesses and write accesses per cycle. *Sevalia*, column 2, lines 18-38 states:

> The circuit 100 may allow users to access and/or control the multiple FIFO storage queues 102a-102n within a single package. Datacom and telecom applications generally need simultaneous access to one or more storage queues (FIFO storage queues 102a-102n). The data in each of the storage queues generally follows the FIFO format (i.e., first-in, first-out). The circuit 100 may allow such access. Additionally, the width and/or depth of the circuit 100 may depend on the architecture of the particular implementation. Without the circuit 100, several separate FIFOS would generally be implemented, each with different data widths and/or depths, to satisfy such requirements. Such a multiple FIFO implementation may cause inventory and other problems described in the background section. The circuit 100 may ease such inventory issues by allowing the user to configure the depth and/or the width of the circuit 100 depending upon a configuration (series and/or parallel) of the storage queues 102a-102n. In such an implementation, only a single device may need to be stocked that may fulfill various design considerations. (*Sevalia*, col. 2, lns. 18-38)

Clearly, column 2, lines 18-38, merely describe the multiple FIFO queues 102a-102n. The multiple FIFO queues (relied upon by the Office Action as the predetermined register memory sections) are included within the circuit 100 (relied upon by the Office Action as the memory). In contrast, independent Claim 1 recites that the buffer memory is coupled to said at least one access port and to said memory. The multiple FIFO queues 102a-102n cannot be the buffer memory since the multiple FIFO queues 102a-102n cannot be both included in the memory and coupled to the memory.

Further, *Sevalia* does not teach or suggest, "wherein a line width of said buffer memory and said memory is selected to be greater or equal the data width of said at least one access port multiplied by the sum of read accesses and write accesses per cycle." *Sevalia* merely teaches, and is limited to teaching, that the circuit may be configured in series or parallel. The cited portions of *Sevalia* contain no disclosure for selecting a line width to be great or equal the dat width of the access port multiplied by the sum of the read accesses and write accesses per cycle. Accordingly, *Sevalia*

does not teach or suggest "a buffer memory coupled to said at least one access port and to said memory, wherein a line width of said buffer memory and said memory is selected to be greater or equal the data width of said at least one access port multiplied by the sum of read accesses and write accesses per cycle" as recited by independent Claim 1.

Accordingly, the Applicants respectfully request that the § 102(e) rejection of Claims 1-2, 4-6, 8 and 10 be withdrawn.

II. ALLOWABLE SUBJECT MATTER

Applicants thanks the Examiner for the indication that Claims 16 and 21 are allowable. The Examiner objected to Claims 3, 9 and 11-15 as being dependent upon a rejected base claim, but suggested that Claims 3, 9 and 11-15 would be allowable if it were rewritten in independent form including all the limitations of the base and intervening claims. Applicants also thank the Examiner for this suggestion but elect not to rewrite Claims 3, 9 and 11-15 at this time.

III. CONCLUSION

As a result of the foregoing, the Applicants assert that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***rmccutcheon@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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